

R423 Stingray

BLOCK DIAGRAM REFLECTING DELL UHMG11 CONFIGURATION.

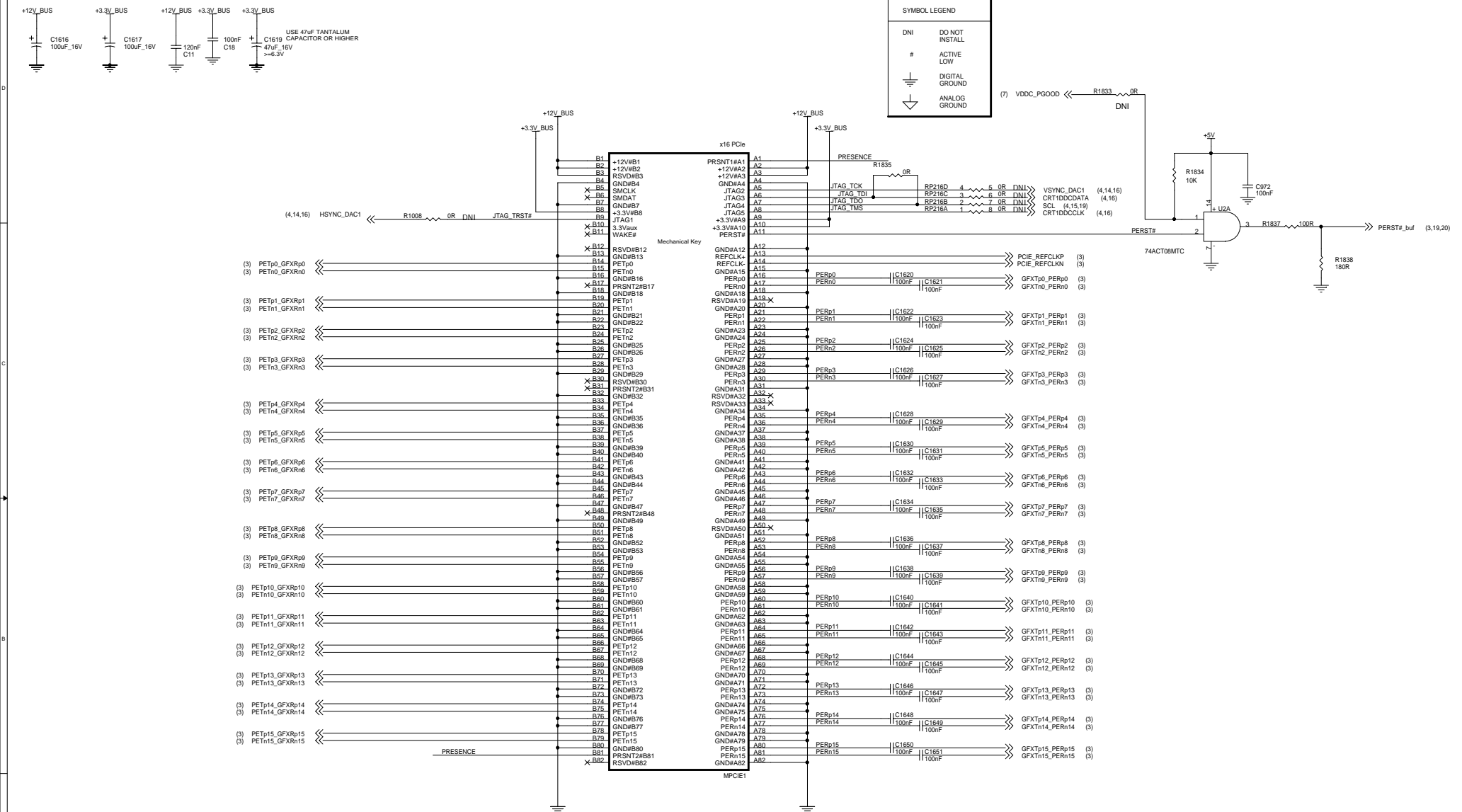
COMPONENTS THAT ARE NOT POPULATED FOR DELL UHMG11 SKU ARE MARKED AS "DNI"



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PCI-EXPRESS EDGE CONNECTOR



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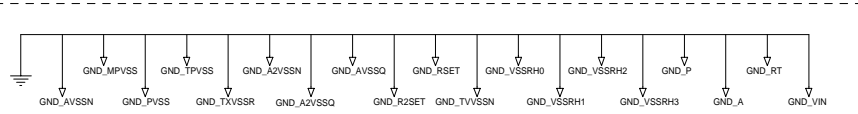
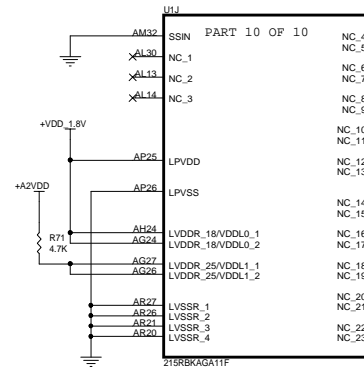
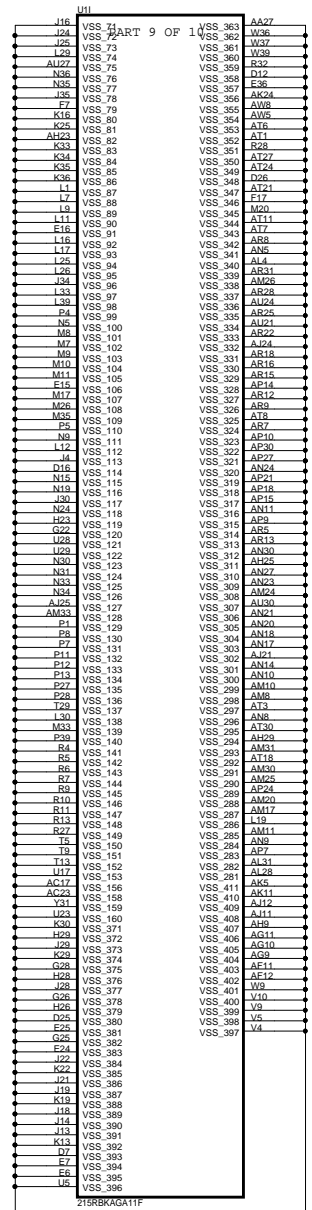
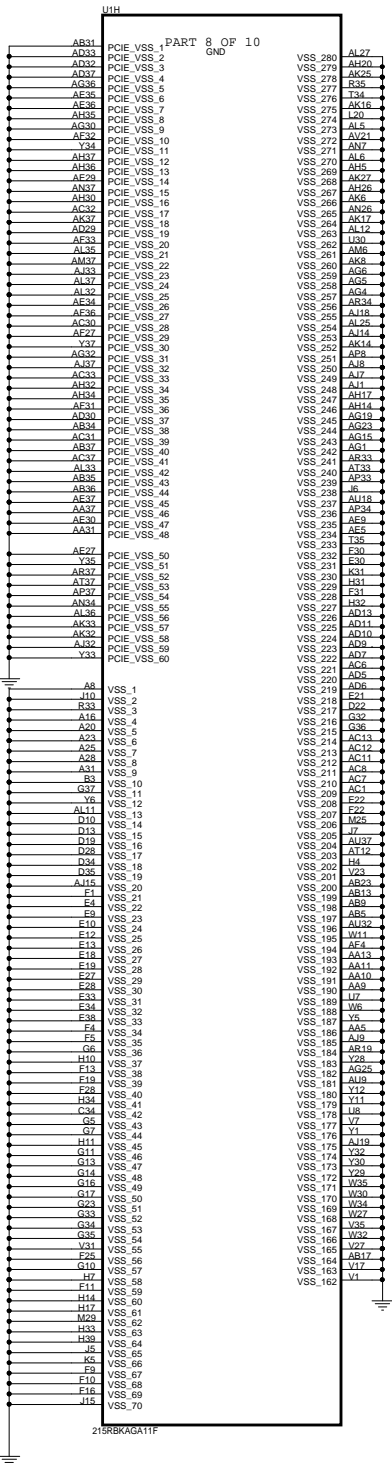
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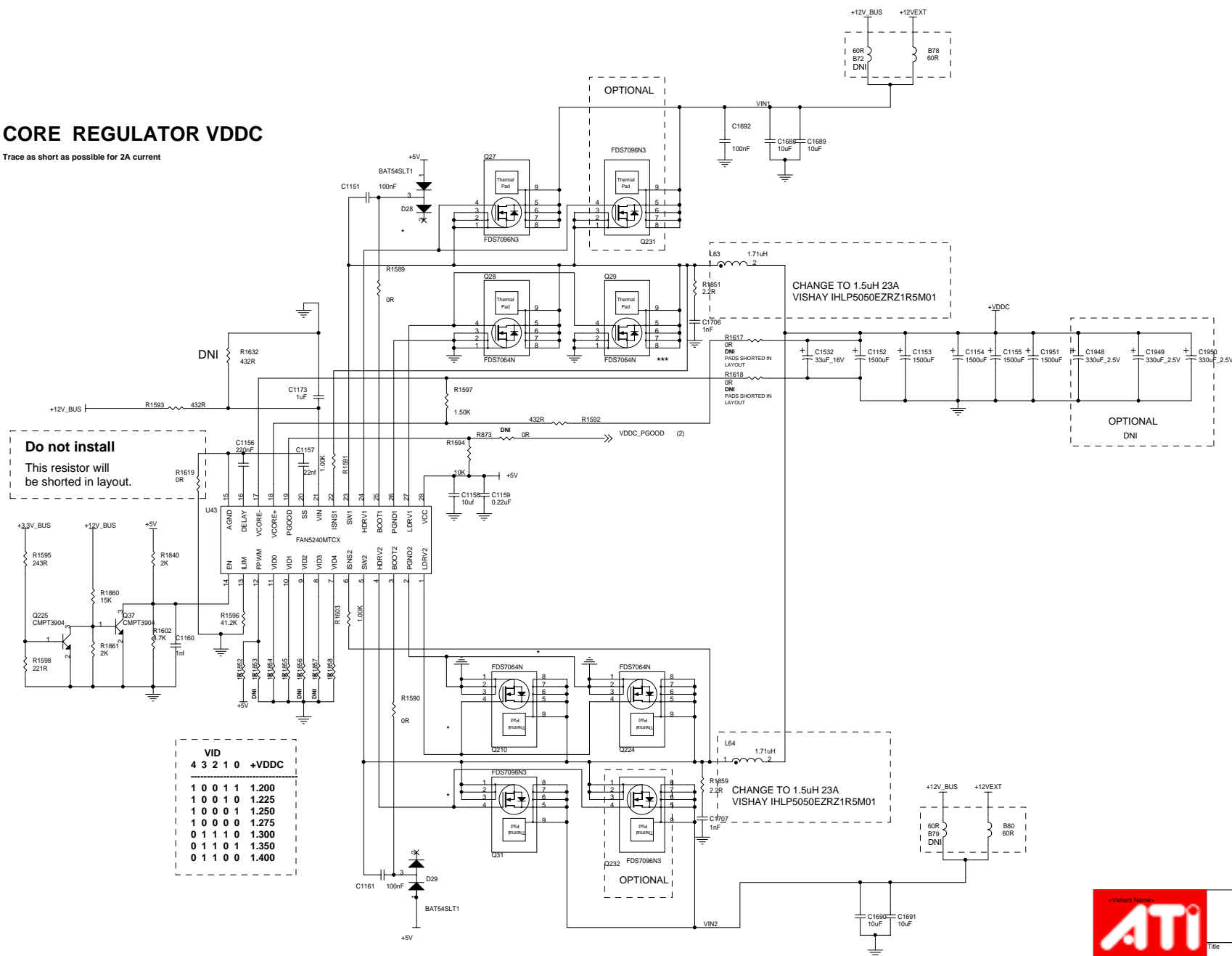
2	1
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Trace as short as possible for 2A current

Do not install
This resistor will
be shorted in layout.

VID					
4	3	2	1	0	+VDDC
1	0	0	1	1	1.200
1	0	0	1	0	1.225
1	0	0	0	1	1.250
1	0	0	0	0	1.275
0	1	1	1	0	1.300
0	1	1	0	1	1.350
0	1	1	0	0	1.400



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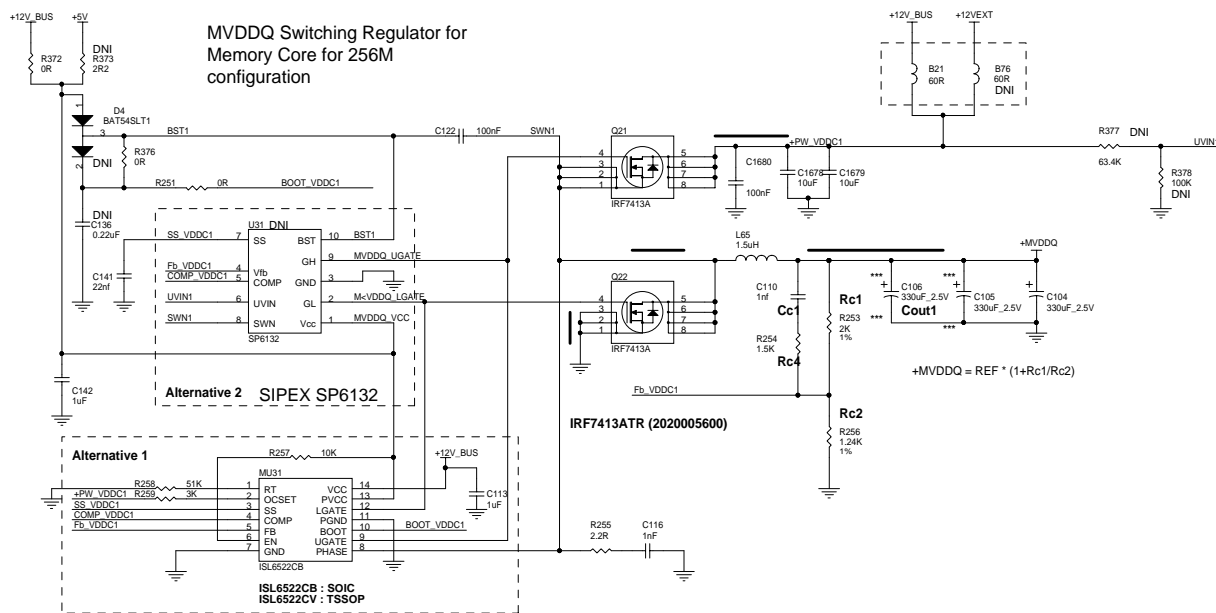
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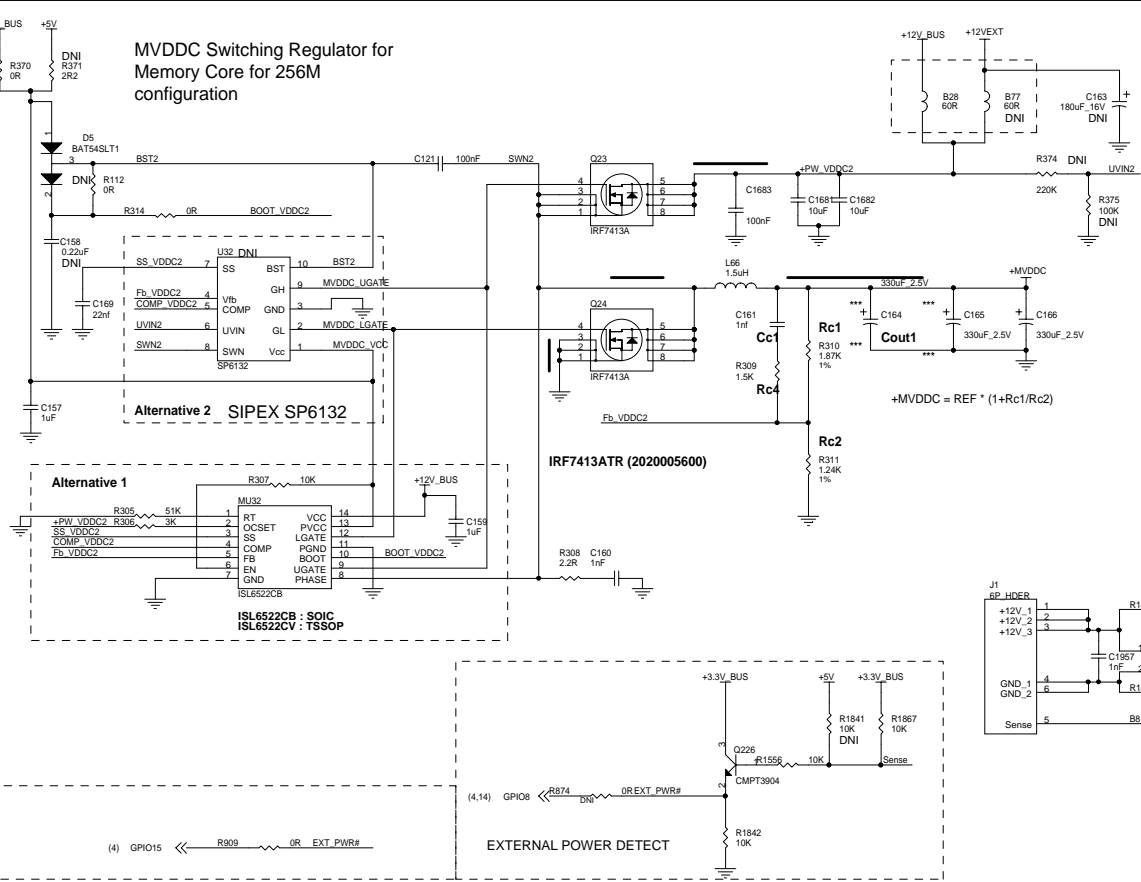
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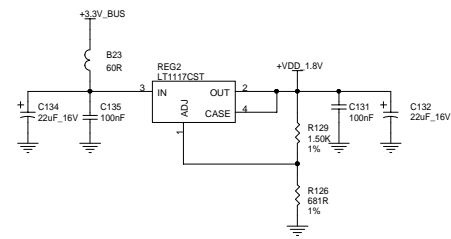
[illegible]



POWER SEQUENCING CIRCUIT:	DESIGN NOTES:
	Add this Capacitor for SP6132
	Compensation Circuit
FOR ALTERNATE #2 Change C142 for 10uF Change C122 for 1uF Replace R251 with a bead Swap Rc4 with Cc1	

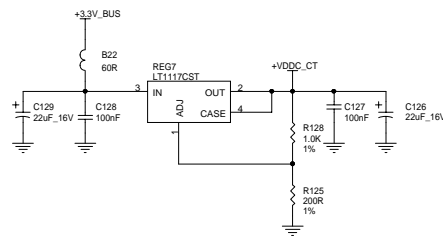


+1.8V Regulator for analog power supplies

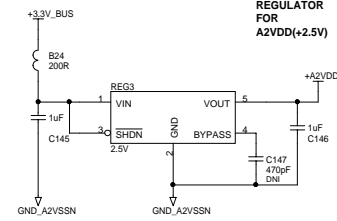


Max 400 mA if all 1.8 V analog power supplies are connected

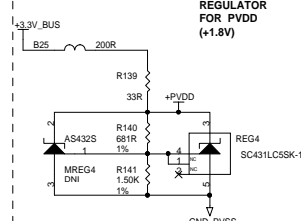
+1.5V Regulator for VDDC_CT (VDD15)



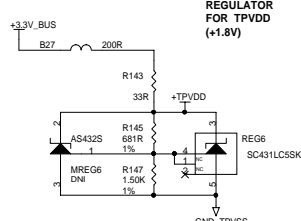
REGULATOR FOR A2VDD(+2.5V)



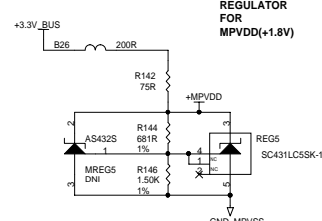
REGULATOR FOR PVDD (+1.8V)



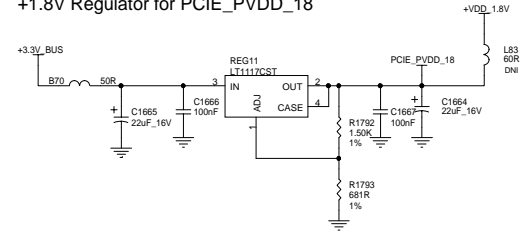
REGULATOR FOR TPVDD (+1.8V)



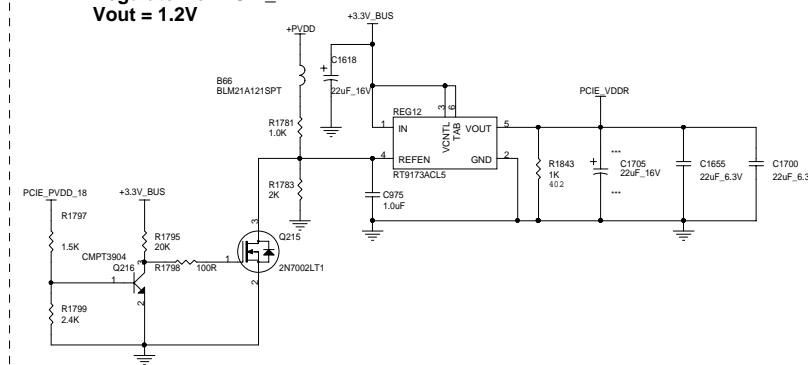
REGULATOR FOR MPVDD(+1.8V)



+1.8V Regulator for PCIE_PVDD_18

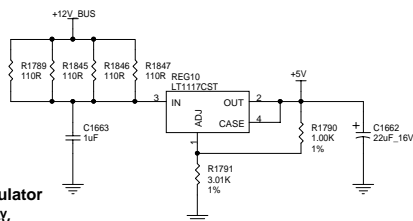


Regulator for PCIE_VDDR Vout = 1.2V



+5V regulator

Vin = 12V
Vout = 5V
Iout =



<Variant Name>



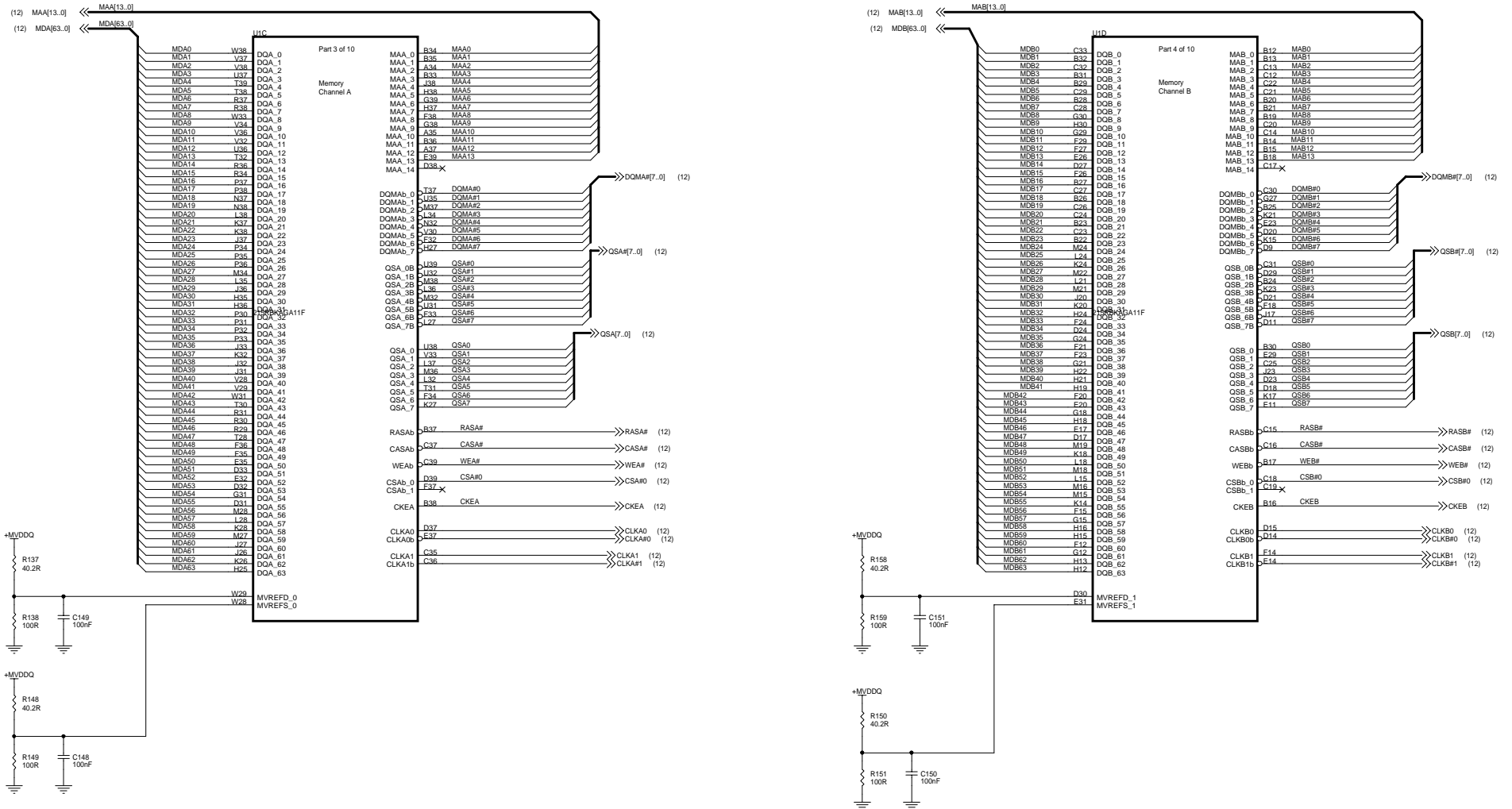
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R423 MEMORY CHANNELS A and B

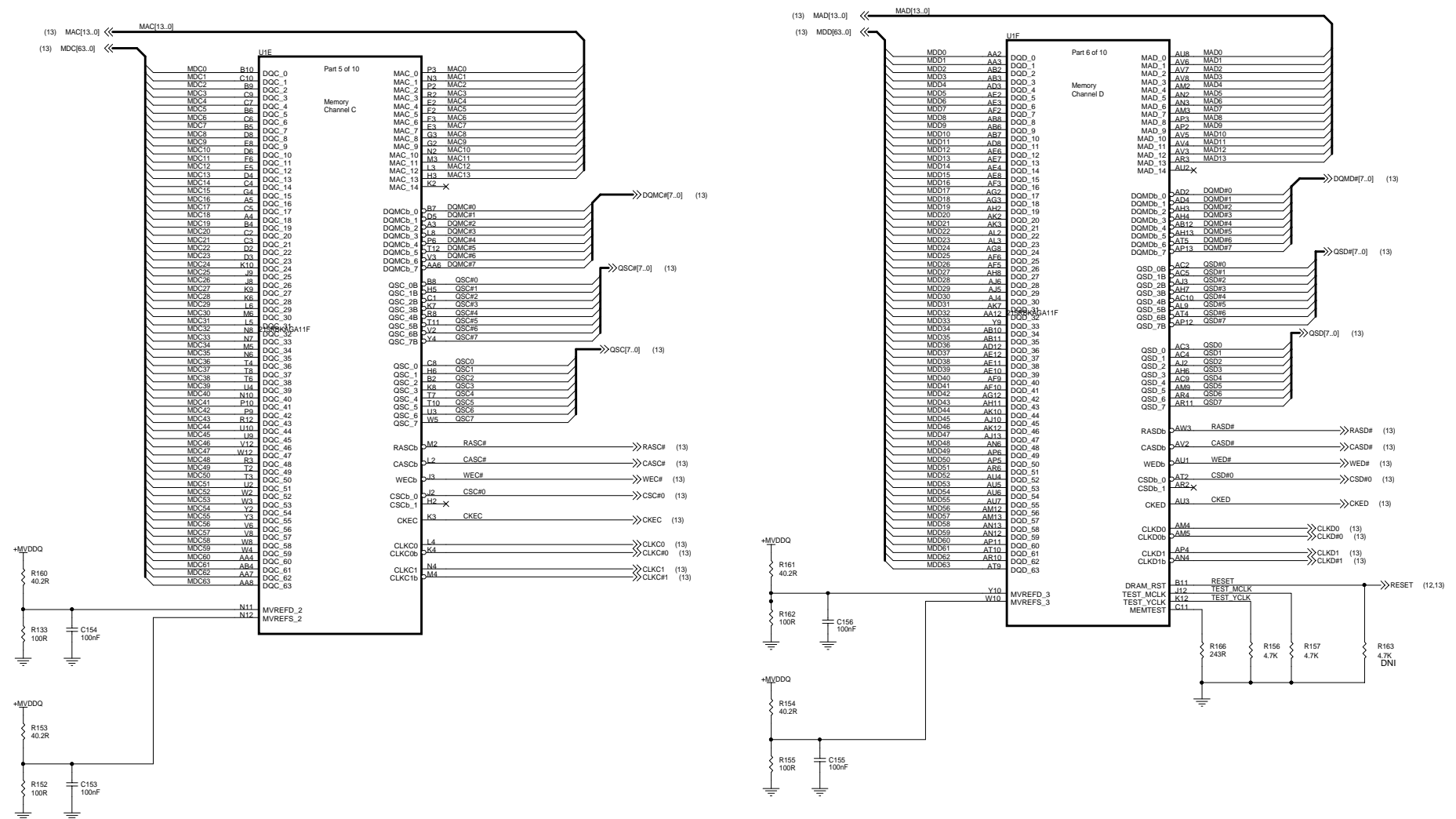


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R-420 MEMORY CHANNELS C and D



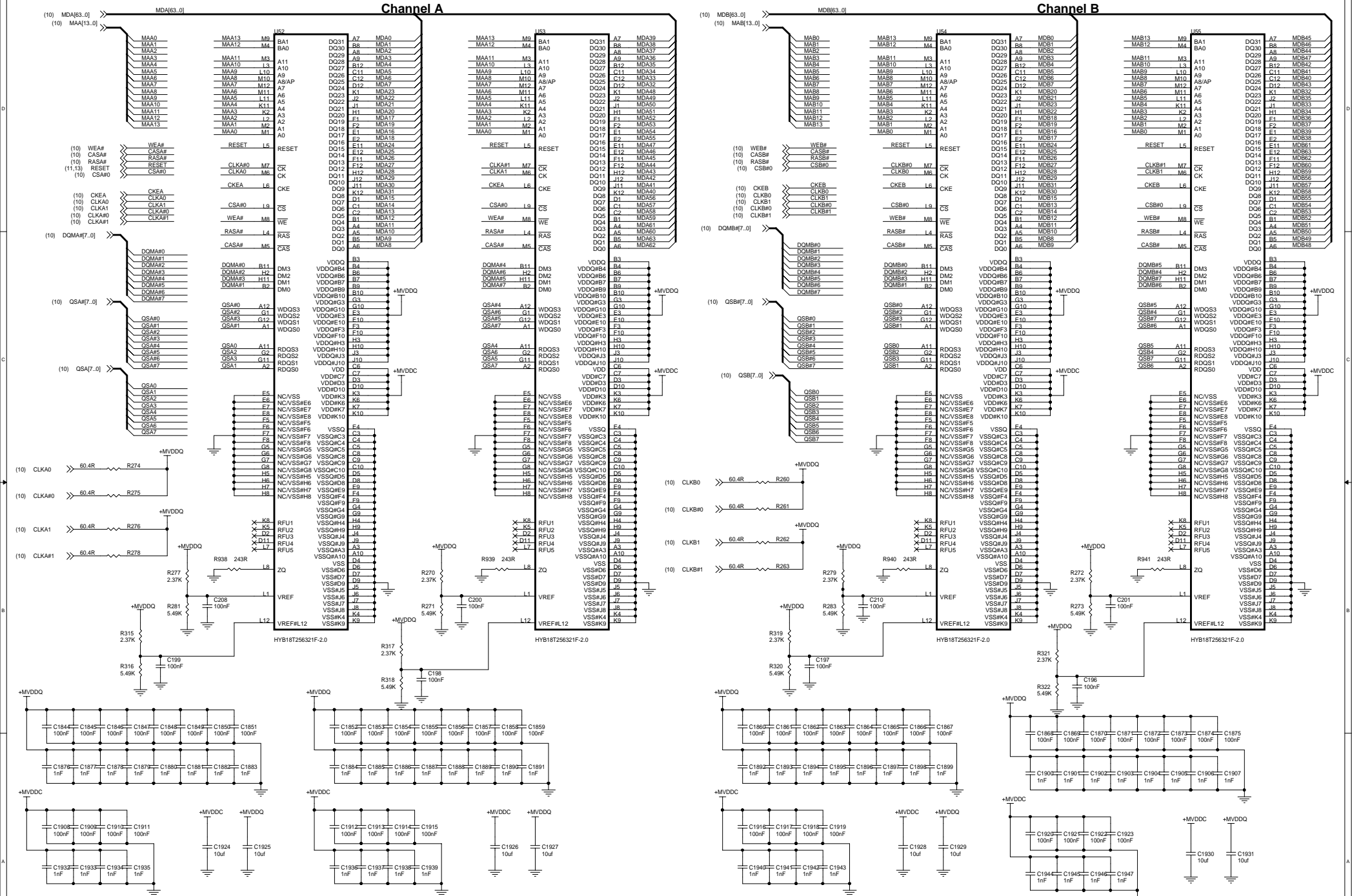
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256 Mbit GDDRIII Channels A and B

Channel A

Channel B



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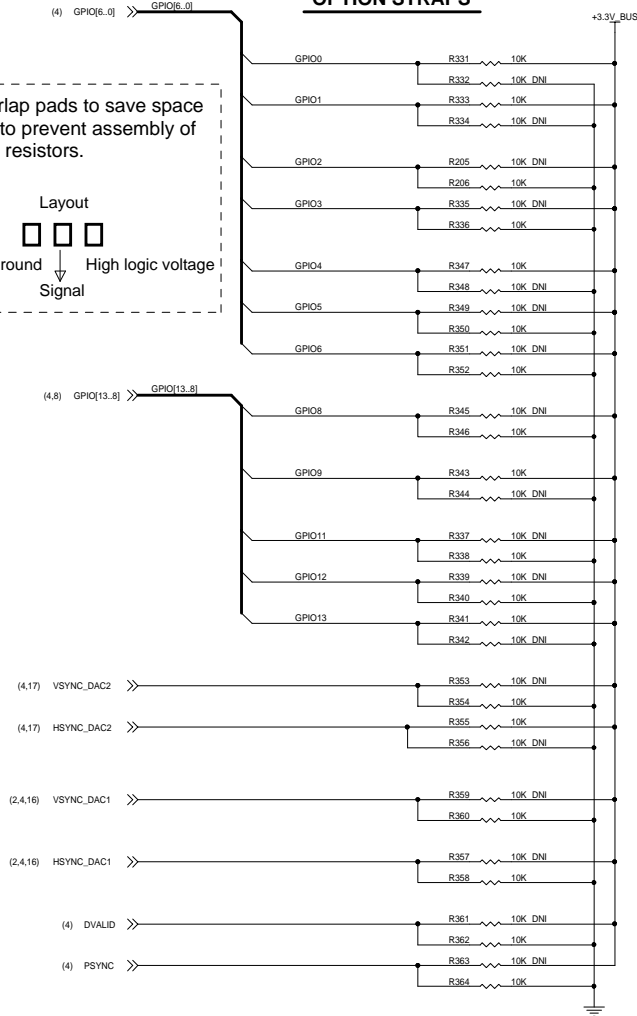
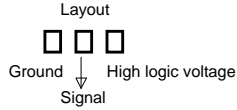
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Channel D



Overlap pads to save space and to prevent assembly of both resistors.



OPTION STRAPS

R423 Shared Straps

REV. 0.0

STRAPS	PIN	DESCRIPTION	DEFAULT
FEATURE0	GPIO(0)	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Desktop must have an external pullup)	0
FEATURE1	GPIO(1)	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Desktop must have an external pullup)	0
PCIE_MODE (ATI Internal)	GPIO(3:2)	PCIE mode: 00: PCI Express 1.0A mode 01: Xyren-compatible mode 10: PCI Express 1.0 mode 11: Short-circuit internal loopback and PCI Express 1.0A mode	00
REVERSE_LANES	GPIO(4)	REVERSE_LANES 0: normal mode 1: reverse mode	0
FORCE_COMPLIANCE	GPIO(5)	Force chip to get to compliance state quickly for Tester purposes 0: Normal operation 1: Force to compliance state	0
PLL_BW (ATI Internal)	GPIO(6)	0: Full PLL Bandwidth 1: Reduced PLL bandwidth	0
DEBUG_ACCESS	GPIO(8)	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible 0: Disable debug access 1: Enable debug access	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDs. If rom attached identifies ROM type. GPIO[9,13,12,11] 000x - No ROM, CHG_ID=00 001x - No ROM, CHG_ID=01 010x - No ROM, CHG_ID=10 011x - No ROM, CHG_ID=11 1001 - 1M Serial AT25F1024 ROM (Atmel) 1010 - 1M Serial AT45DB011 ROM (Atmel) 1011 - 1M Serial M25P10 ROM (ST) 1100 - 512K Serial M25P05 ROM (ST) 1101 - 1M Serial SST45LF010 ROM (SST) 1M Serial W45B512 ROM (WinBond) 512K Serial W45B012 ROM (WinBond) 1110 - 1M Serial SST25VF010 ROM (SST) 512K Serial SST25VF512 ROM (SST) 1111 - 1M NX25F011B ROM (NexFlash) Chip IDs: Chip ID is based on substrate fuses and CHG_ID strap (which comes from ROM if used, or pin straps if no ROM is connected): CHG_ID = ROMIDCFG[2:1] = GPIO[13:12]	1100
MULTIFUNC(1:0)	H2SYNC, V2SYNC	Multi-function device select. 00 - single function device. 01 - two function device. 10 - two function device. 11 - two function device.	10
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this in low during reset. 0 - Slave VIP host port devices present 1 - No slave VIP host port devices reporting presence during reset	1
RFU	HSYNC	RFU 0 - Normal 1 - Not used	0

R423 Dedicated Straps

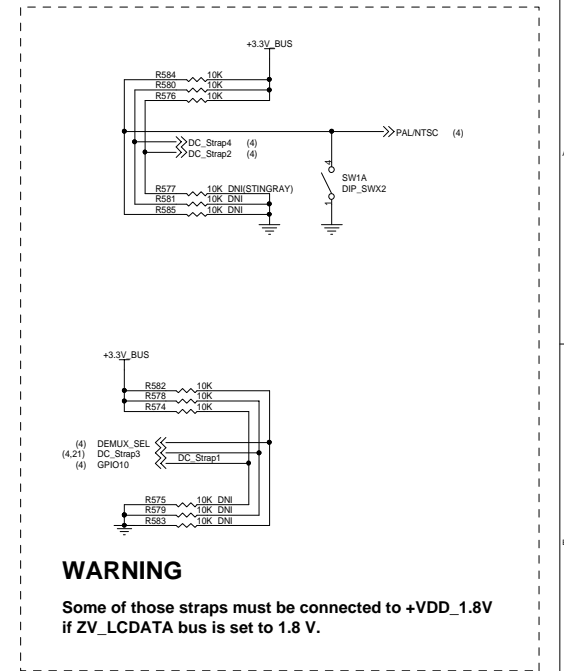
REV. 0.0

ZV_VOLTAGE_SEL0	DVOVMODE_0	DVOVMODE_0 is for ZV_LCDCNTL and ZV_LCDDATA(11:0). 0 - 3.3 V signaling 1 - 1.8 V signaling	0
ZV_VOLTAGE_SEL1	DVOVMODE_1	DVOVMODE_1 is for ZV_LCDDATA(23:12) 0 - 3.3 V signaling 1 - 1.8 V signaling	0

Board Straps

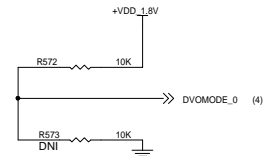
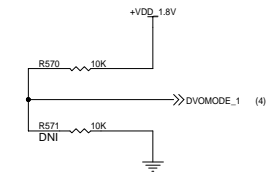
REV. 0.0

STRAPS	PIN	DESCRIPTION	DEFAULT
MEMTYPE(1:0)	DVALID, PSYNC.	Memory connected to R420 identification for BIOS 00 - Samsung GDDR 3 memory 144 Ball BGA package 01 - TBD 10 - TBD 11 - TBD	000
DC_Strap1	GPIO(10)	Internal TMD5 Enabled 0 - Disabled 1 - Enabled	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled 0 - Disabled 1 - Enabled	0
DC_Strap3	LCDDATA(14)	Not defined	0
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off 01 - DAC2 On as CRT 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PALNTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) 0 - PAL (on board resistor pull-down and switch closed) 1 - NTSC (on board resistor pull-up)	1
EXT_PWR	GPIO15	External power cable detect 0 - Cable is properly connected 1 - Cable is not properly connected. Software should prevent the board from booting, should display a warning at screen and should decrease engine and memory clock speed.	NA



WARNING

Some of those straps must be connected to +VDD_1.8V if ZV_LCDDATA bus is set to 1.8 V.



<Variant Name>



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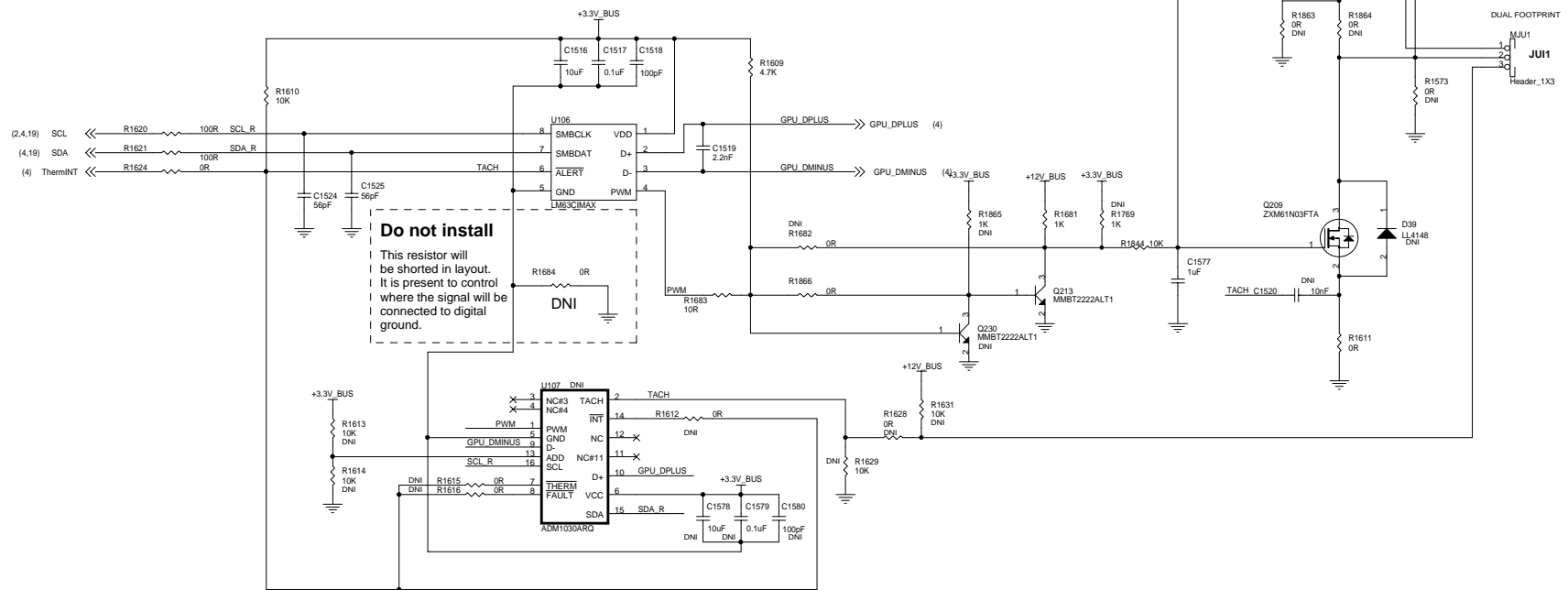
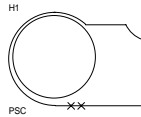
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TEMPERATURE SENSE AND SPEED CONTROLLED FAN

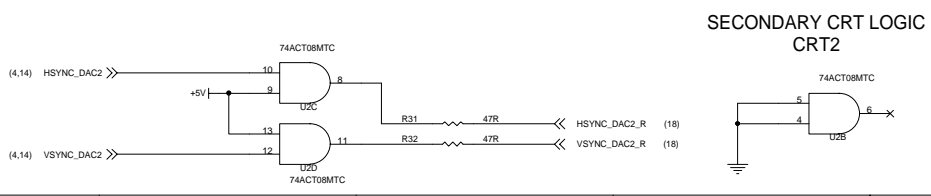
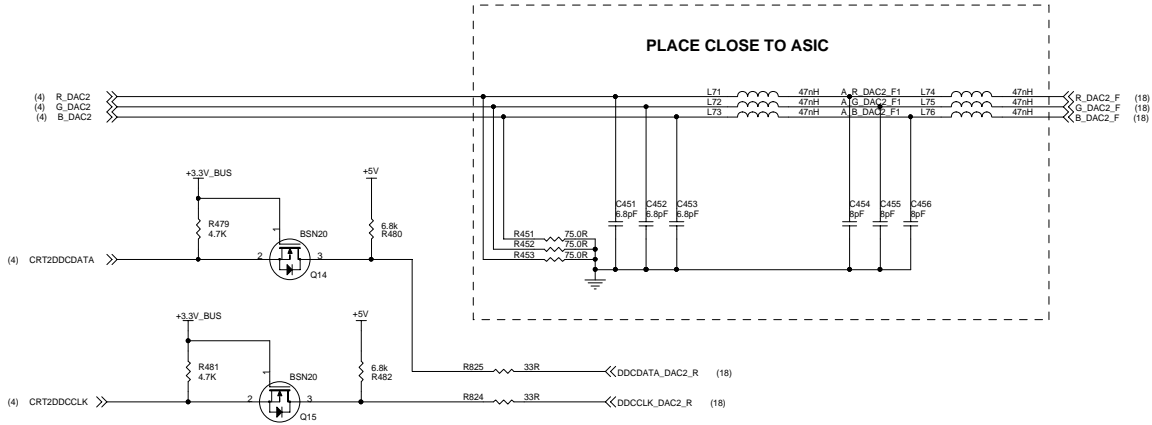
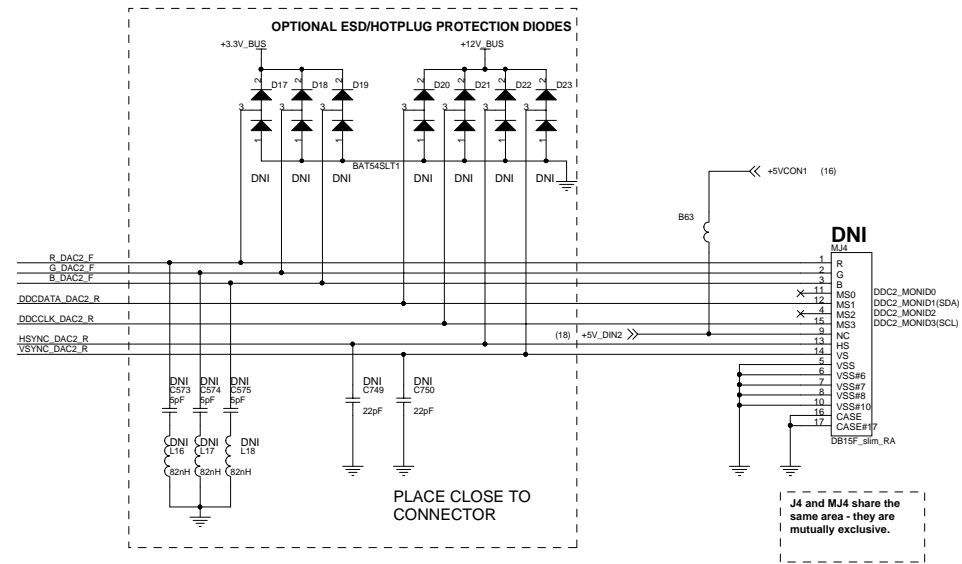


Change to Maxim part

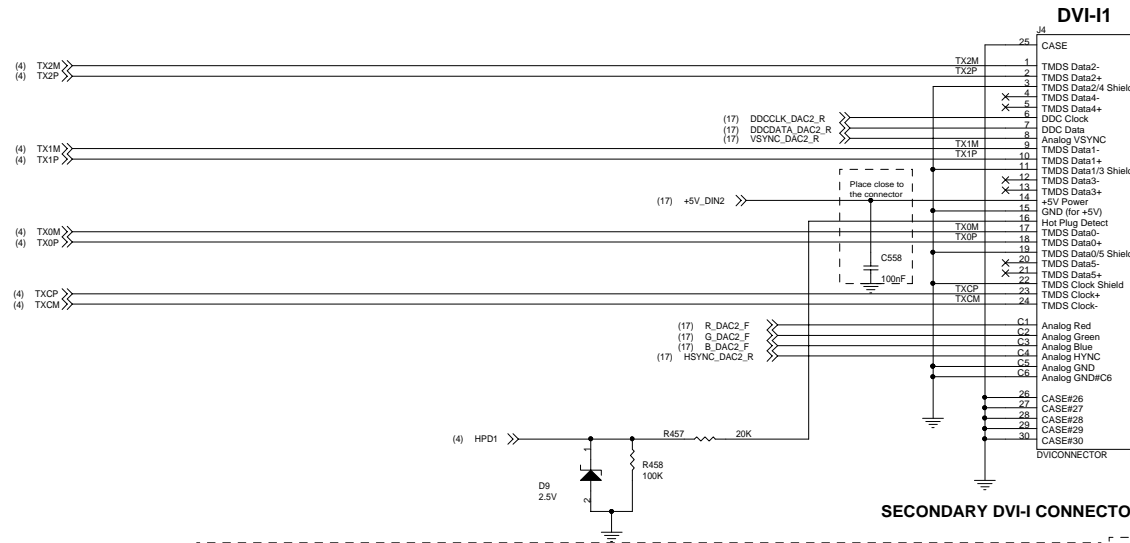


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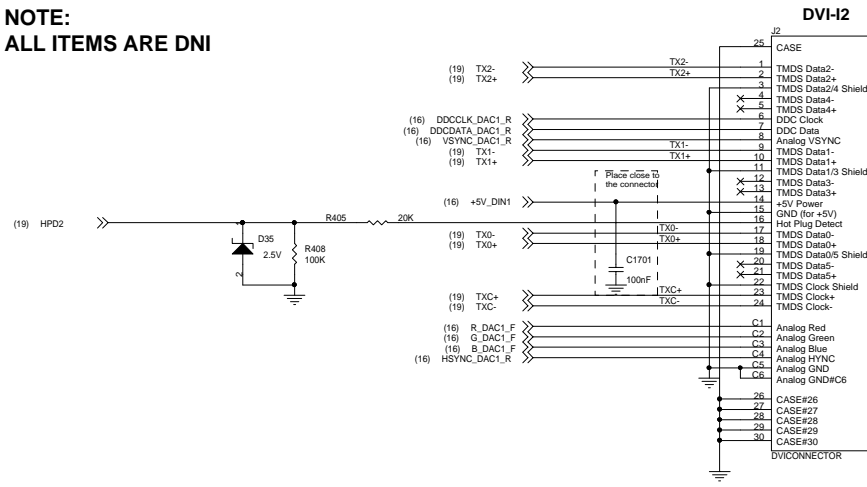


PRIMARY DVI-I CONNECTOR (DVI-I1)



SECONDARY DVI-I CONNECTOR

NOTE:
ALL ITEMS ARE DNI



J2 and MJ2 share the same area - they are mutually exclusive.



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**NOTE:
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PAGE ARE ALL DNI**



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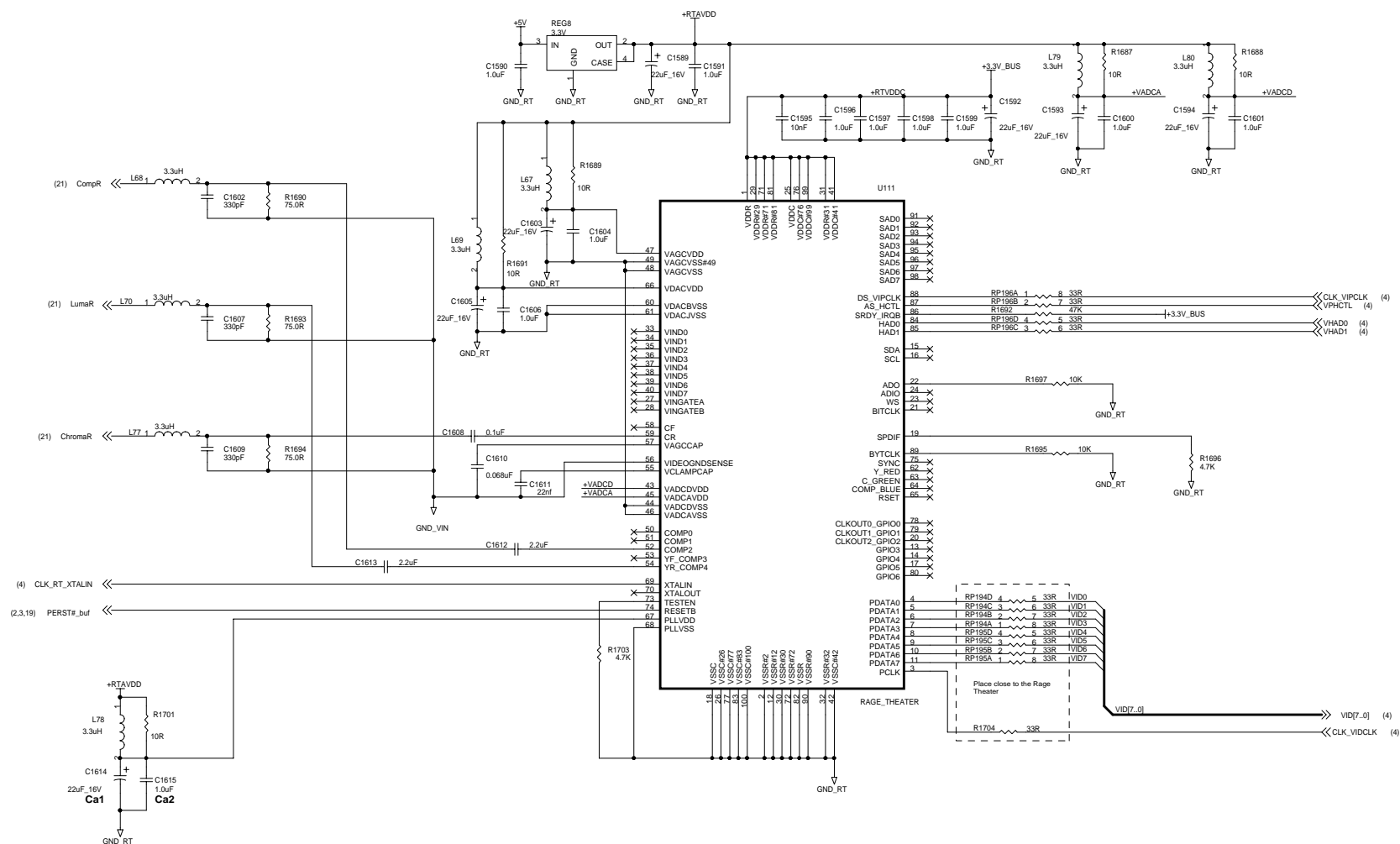
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NOTE:
ITEMS ON THIS
PAGE ARE ALL DNI



IMPORTANT

Layout Guide line of THEATER

- #1 : Ca1 and Ca2 have to be placed as close as possible to the respective pins of Rage THEATER
- #2 : GND_VIN should be separated from Digital or Chassis Ground and have no loops
- #3 : GND_VIN should be connected to Digital GND plane at one point as close as possible to pin 56 of THEATER

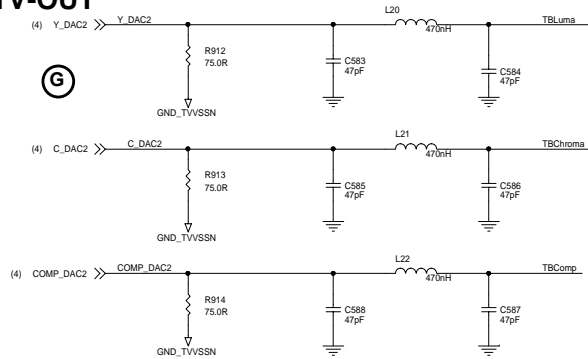
Put 2D line as close as possible to pin 56 of Rage Theater



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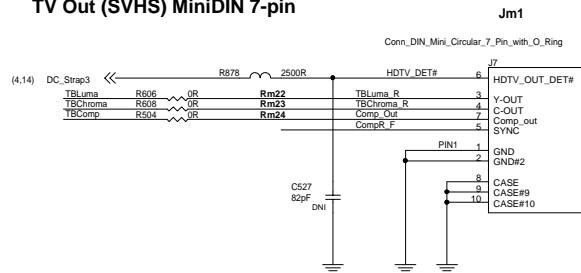
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TV-OUT

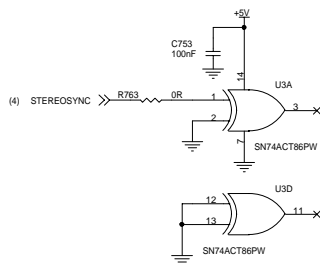


Footprint - M1

TV Out (SVHS) MiniDIN 7-pin



Connector Jm1 uses the same footprint as Jm2 and Jm3

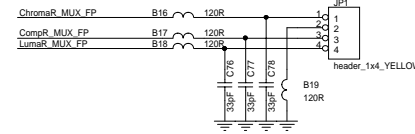


NOTE:
ALL ITEMS ARE DNI

(C)

Connector Jm2 uses the same footprint as Jm1 and Jm3

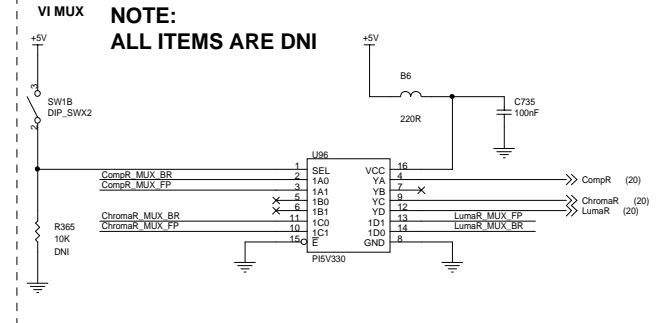
NOTE:
ALL ITEMS ARE DNI



VI MUX BYPASS DNI

NOTE:
ALL ITEMS ARE DNI

NOTE:
ALL ITEMS ARE DNI



	Install	DNI
TV-OUT 7-PIN MiniDIN 102-00302-00 102-00305-00	(A) (B) (E)	(C)
VIVO 9-PIN MiniDIN 102-00303-00 102-00306-00	(C)	(A) (B) (E)
No Options (Just DB15)		(A) (B) (C) (E)

(A) (C) share the same footprint

<Variant Name>

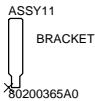
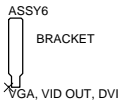
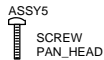
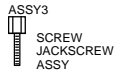
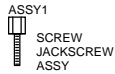


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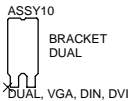
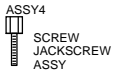
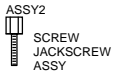
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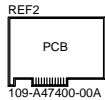
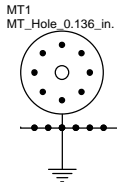
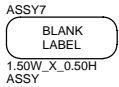
DVI SCREWS



DVI SCREWS



MISC. BOARD PARTS



<Variant Name>



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Title

PCIe R480 GDDR3 256MB 8MX32 DVI-I DVI-I

Schematic No.

105-A474XX-10

Date:

Thursday, November 11, 2004

REVISION HISTORY

Rev 2

Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	13/06/04	Initial revision of the schematic based on 105-A319xx-00: - Added decoupling caps for GDDR3 memory devices
1	00	12/10/04	- Separated VDDC input power to VIN1 and VIN2 (added B and B) - Added HPD2_INT for the second DVI connector (using ext TMDS)
2	10	11/11/04	- PCB change only: extended gnd on layer 10 to ensure connection to fan screws - No electrical changes.